



## **40G QSFP+ SR2-BiDi Transceiver** **Hot Pluggable, Dual Bidi LC, 850 / 908nm VCSEL, MMF 100M, DDM**

**Part Number: FQFP- IC-C85-X1D**



### **Overview**

FQFP-IC-C85-X1D is a pluggable optical transceiver with a Dual Bidi LC connector for short-reach 40G data communication and interconnect applications using multi-mode fiber. It allows reuse existing 10G duplex MMF cabling Infrastructure for easy migration to 40 Gigabit Ethernet connectivity. The transceiver internally multiplexes XLPPi 4x10G interface into 2x20G electrical channels, then converting to 2x20G optical channels for an aggregated data rate of 40G up to MMF OM3 100m optical link.

### **Applications**

- 40GBASE-SR2 Ethernet @41.3G
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

### **Features**

- Compliant with 40GBASE-SR2 BiDi
- Compliant with SFF-8436 QSFP+ MSA
- Compliant with IEEE 802.3ba-2010 40GbE XLPPi Interface
- Dual wavelength 850 / 908nm VCSEL Bi-Directional optical interface
- Up to 11.2Gbps data rate per 10G channel
- Built in quad TX CDR and RX CDR
- Hot Pluggable
- Dual Bidi LC connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8436, SFF-8636
- Single 3.3V power supply
- Link distance 100m over OM3 fiber and 150m over MM OM4 fiber
- Maximum power consumption 3.5W
- RoHS compliant



## Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.

## Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T <sub>ST</sub>	-40	+85	°C
Storage Relative Humidity	RH	0	85	%
Supply Voltage	V <sub>CC3</sub>	-0.5	+3.6	V

## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T <sub>OP</sub>	0	-	+70	°C
Supply Voltage	V <sub>CC</sub>	+3.13	+3.3	+3.47	V
Electrical Data Rate, per Lane	DR <sub>EL</sub>		10.3125	11.2	Gb/s
Data Rate Accuracy	ΔDR	-100		+100	ppm
Bit Error Rate ( NO FEC )	BER			5x10 <sup>-5</sup>	
Supply Current	I <sub>CC</sub>		750	1000	mA
Power Consumption	P		2.5	3.5	W
Transceiver Power-on Initialization Time				2000	ms
Control Input Voltage High	V <sub>IH</sub>	2.0		V <sub>CC</sub>	V
Control Input Voltage Low	V <sub>IL</sub>	GND		0.7	V
Control Output Voltage High	V <sub>OH</sub>	2.0		V <sub>CC</sub>	V
Control Output Voltage Low	V <sub>OL</sub>	GND		0.7	V



## Transmitter Electro-optical Characteristics

$V_{CC} = 3.13V$  to  $3.47V$ ,  $T_{OP} = 0\text{ }^{\circ}C$  to  $70\text{ }^{\circ}C$

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Optical Channel	DR <sub>OP-T</sub>		20.625		Gb/s	
Average Launch Power, per Channel	P <sub>AVG</sub>	-4	-2.5	+5	dBm	
Optical Wavelength, CH1	$\lambda_{CH1}$	832	850	868	nm	1
Optical Wavelength, CH2	$\lambda_{CH2}$	882	908	918	nm	1
Spectral Width (RMS)	$\Delta\lambda$		0.5	0.65	nm	1
Optical Extinction Ratio	ER	3			dB	
Average Launch Power OFF, per Channel	P <sub>OFF</sub>			-30	dBm	
Optical Return Loss Tolerance	ORLT			12	dB	
Input Differential Impedance	Z <sub>IN</sub>	80	100	120	$\Omega$	
Differential Data Input Voltage	V <sub>IN-PP</sub>	120		1200	mVpp	

**Note1:** Transmitter wavelength, RMS spectral width and launch power need to meet the OMA minus TDP specs to guarantee link performance.



## Receiver Electro-optical Characteristics

$V_{CC} = 3.13V$  to  $3.47V$ ,  $T_{OP} = 0\text{ }^{\circ}C$  to  $70\text{ }^{\circ}C$

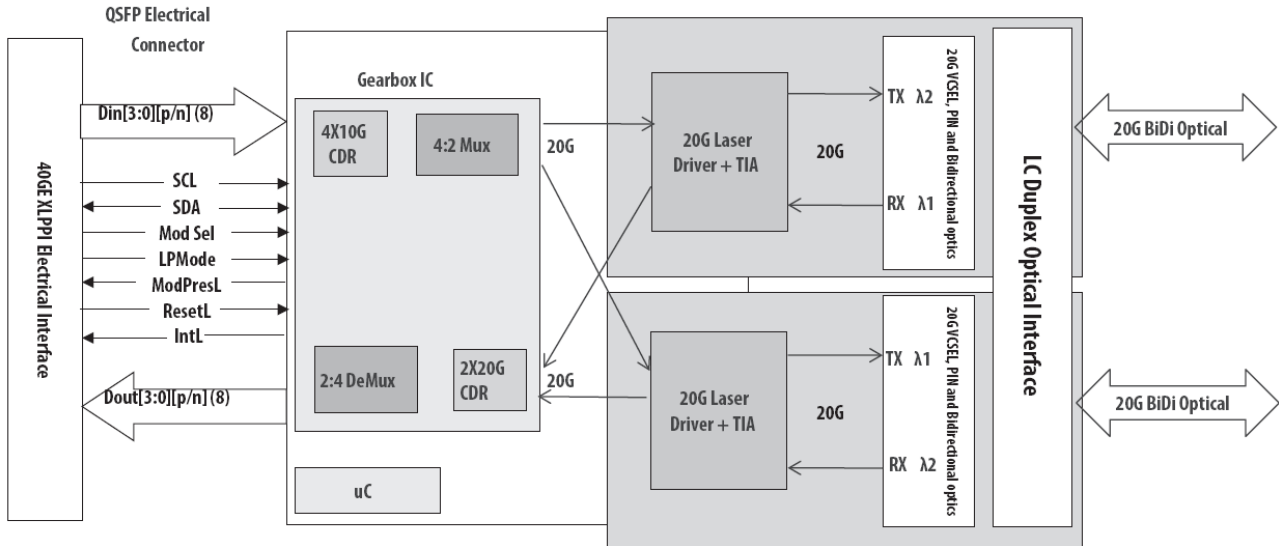
Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Optical Channel	DR <sub>OP-R</sub>		20.625		Gb/s	
Maximum Receive Power, per Channel	P <sub>RX-MAX</sub>	+5			dBm	1
Receiver Sensitivity, per Channel	SEN			-6.5	dBm	2
Optical Wavelength, CH1	$\lambda_{CH1}$	882	908	918	nm	
Optical Wavelength, CH2	$\lambda_{CH2}$	832	850	868	nm	
Receiver Reflectance	R <sub>RX</sub>			-12	dB	
LOS De-Assert	LOS <sub>D</sub>			-8.6	dBm	
LOS Assert	LOS <sub>A</sub>	-30	-14		dBm	
LOS Hysteresis	LOS <sub>HY</sub>	0.5			dB	
Output Differential Impedance	Z <sub>OUT</sub>	80	100	120	$\Omega$	
Differential Data Output Voltage	V <sub>OUT-PP</sub>	300	600	800	mVpp	

**Note1:** The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

**Note2:** Measured with conformance test signal at receiver input for BER=  $5 \times 10^{-5}$ .



## Transceiver Block Diagram



## Pin Assignment

38	GND
37	Tx1n
36	Tx1p
35	GND
34	Tx3n
33	Tx3p
32	GND
31	LP Mode
30	Vcc1
29	VccTx
28	IntL
27	ModPrsL
26	GND
25	Rx4p
24	Rx4n
23	GND
22	Rx2p
21	Rx2n
20	GND

Top Side  
Viewed From Top

Module Card Edge

GND	1
Tx2n	2
Tx2p	3
GND	4
Tx4n	5
Tx4p	6
GND	7
ModselL	8
ResetL	9
VccRx	10
SCL	11
SDA	12
GND	13
Rx3p	14
Rx3n	15
GND	16
Rx1p	17
Rx1n	18
GND	19

Bottom Side  
Viewed From Bottom



## Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMODE	Low Power Mode
32		GND	Module Ground

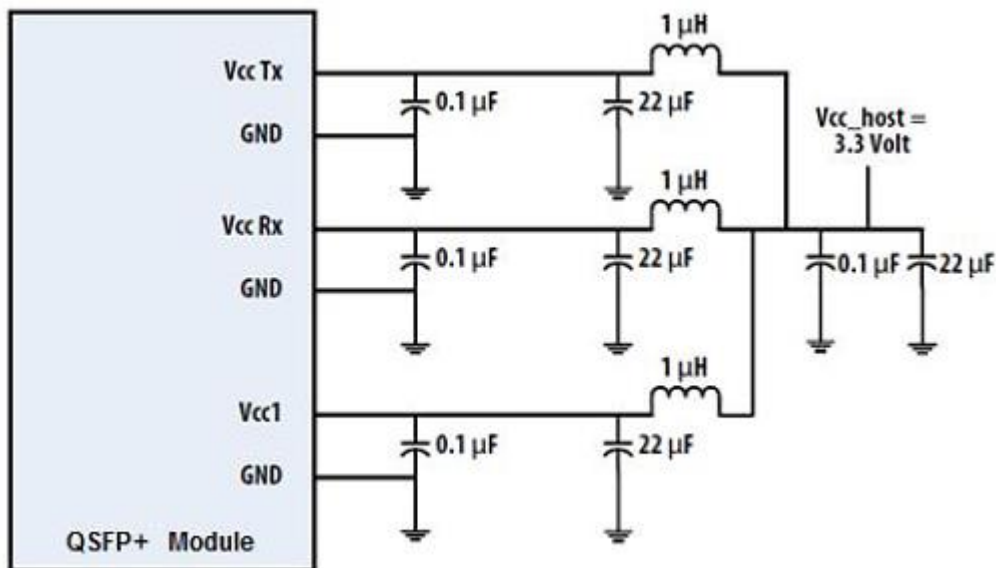


33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

**Note1:** GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

**Note2:** VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

### Recommended Power Supply Filter





## Digital Diagnostic Functions

As defined by the QSFP+ MSA, Ficer's QSFP+ transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

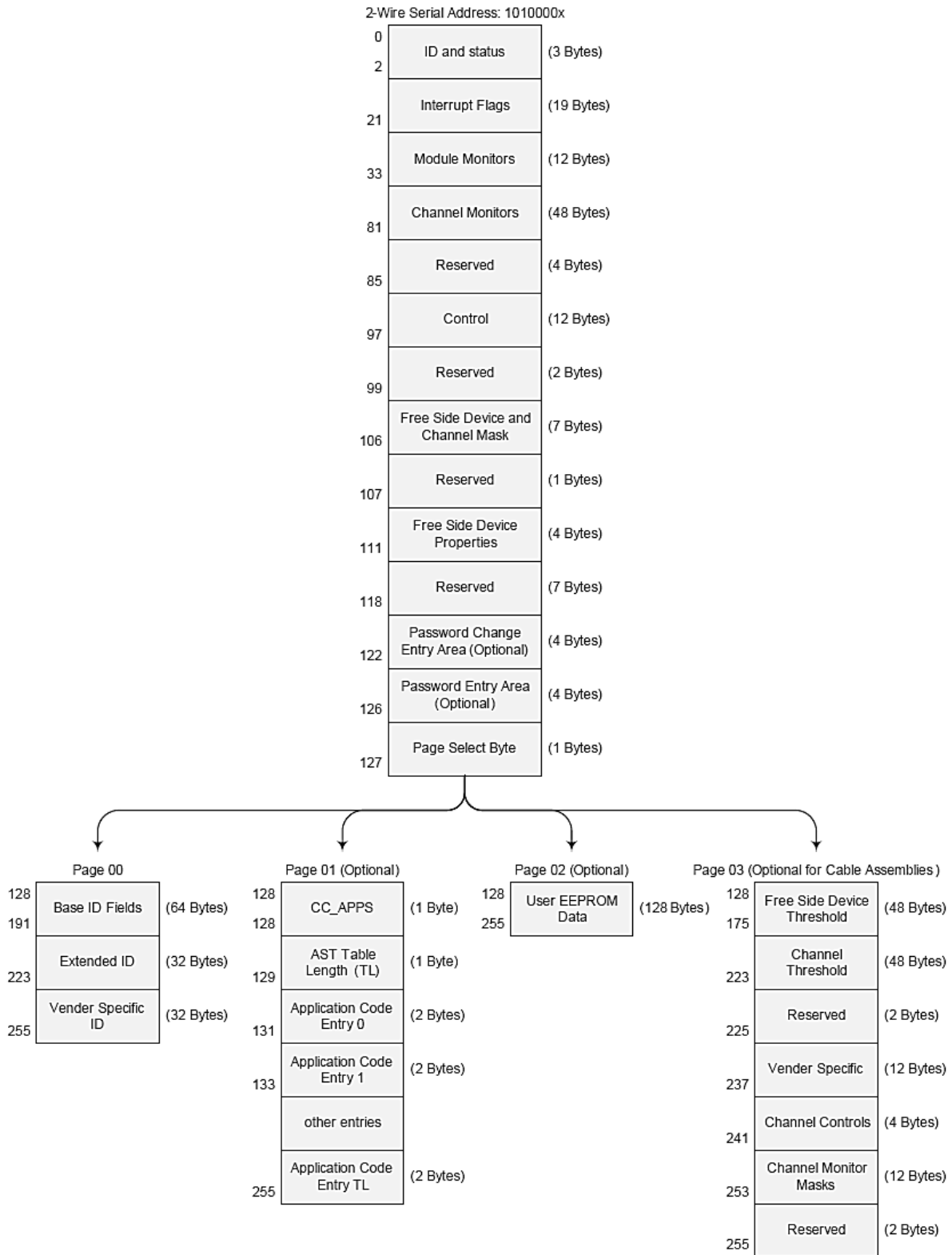
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP+ MSA Specification.

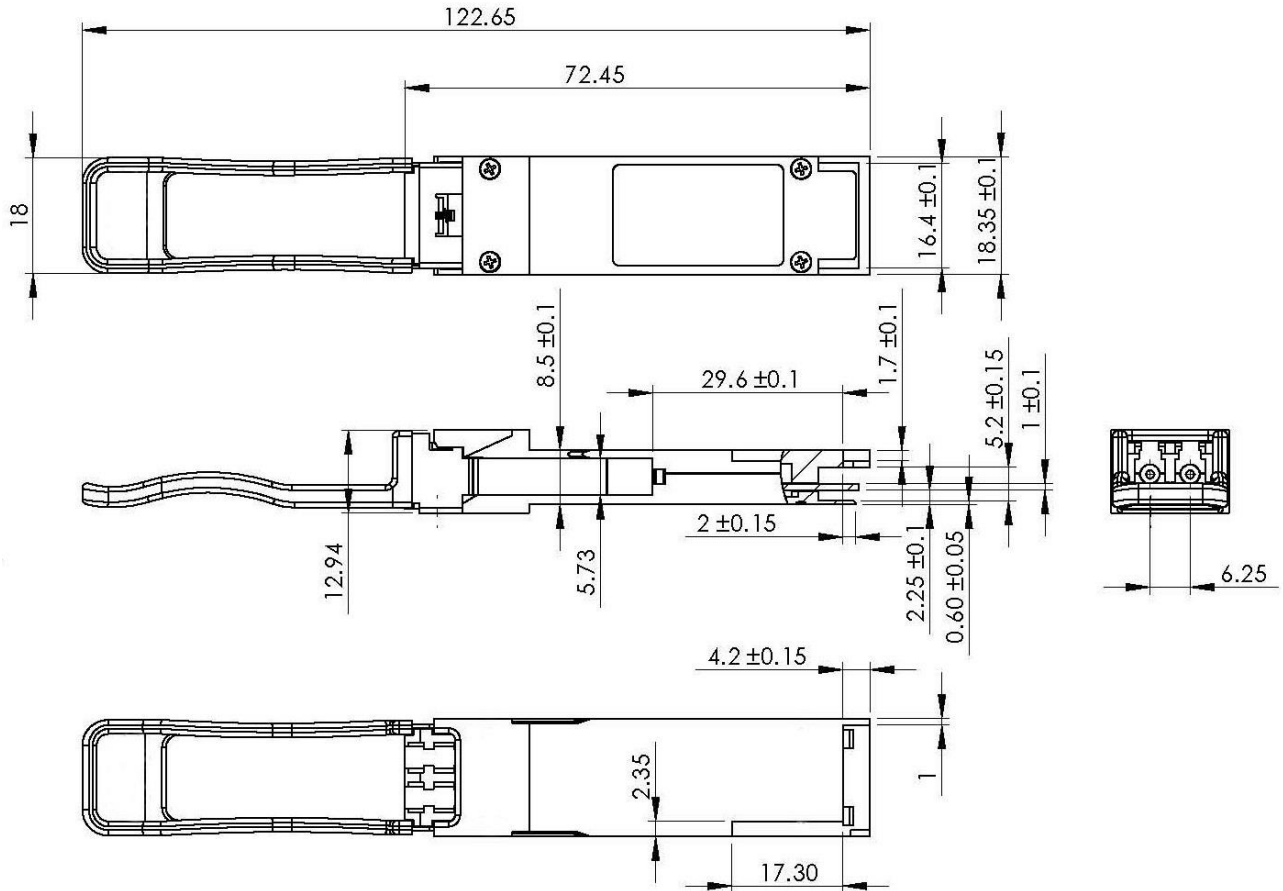
## Digital Diagnostic Memory Map







## Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

## Ordering Information

Part No.	Tx	Rx	Link	DDM	Temp.
FQFP-IC-C85-X1D	850nm 908nm	908nm 850nm	MM OM3 100m MM OM4 150m	Yes	0~70°C

**Note:** Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.